Adders’ states, operands of each state and their select signals:

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Adder 1 | | | | | Adder2 | | | | |
| State1 | Op1 | Op2 | S1a | S1b | State2 | Op1 | Op2 | S2a | S2b |
| A1\_IDLE (0) | - | - | ’b111 | ’b111 | A2\_IDLE (0) | - | - | ‘b111 | ‘b111 |
| A1\_E2 (2) | !E2 | 1 | ’b000 | ’b000 | A2\_2E1\_E3 (1) | 2E1 | E3 | ‘b000 | ‘b000 |
| A1\_2E2 (3) | !2E2 | 1 | ‘b001 | ‘b000 | A2\_E1\_2E3 (3) | E1 | 2E3 | ‘b001 | ‘b001 |
| A1\_E2\_2E3 (1) | E2 | 2E3 | ‘b011 | ‘b001 | A2\_2E2\_E3 (2) | 2E2 | E3 | ‘b011 | ‘b000 |
| A1\_E2\_2E4 (4) | E2 | 2E4 | ‘b011 | ‘b011 | A2\_2E2\_E4 (4) | 2E2 | E4 | ‘b011 | ‘b011 |
| A1\_2E2\_5E4 (5) | -2E2 | 5E4 | ‘b010 | ‘b010 | A2\_5E4 (5) | 4E4 | E4 | ‘b010 | ‘b011 |
| A1\_2E3\_E1 (8) | 2E3 | E1 | ‘b110 | ‘b110 | A2\_4E4\_E2 (7) | 4E4 | -E2 | ‘b010 | ‘b010 |
| A1\_2E3 (12) | !2E3 | 1 | ‘b100 | ‘b000 | A2\_E3 (8) | !E3 | 1 | ‘b110 | ‘b110 |
| A1\_5E1\_2E3 (14) | 5E1 | -2E3 | ‘b101 | ‘b100 | A2\_4E1\_E3 (10) | 4E1 | -E3 | ‘b100 | ‘b100 |
|  |  |  |  |  | A2\_5E1 (11) | 4E1 | E1 | ‘b001 | ‘b100 |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Adder 1 | | | Adder 2 | | |
| State1 | S1a | S1b | State2 | S2a | S2b |
| A1\_IDLE (0) | ’b111 | ’b111 | A2\_IDLE (0) | ‘b111 | ‘b111 |
| A1\_E2 (2) | ’b000 | ’b000 | A2\_2E1\_E3 (1) | ‘b000 | ‘b000 |
| A1\_2E2 (3) | ‘b001 | ‘b000 | A2\_E1\_2E3 (3) | ‘b001 | ‘b001 |
| A1\_E2\_2E3 (1) | ‘b011 | ‘b001 | A2\_2E2\_E3 (2) | ‘b011 | ‘b000 |
| A1\_E2\_2E4 (4) | ‘b011 | ‘b011 | A2\_2E2\_E4 (4) | ‘b011 | ‘b011 |
| A1\_2E2\_5E4 (5) | ‘b010 | ‘b010 | A2\_5E4 (5) | ‘b010 | ‘b011 |
| A1\_2E3\_E1 (8) | ‘b110 | ‘b110 | A2\_4E4\_E2 (7) | ‘b010 | ‘b010 |
| A1\_2E3 (12) | ‘b100 | ‘b000 | A2\_E3 (8) | ‘b110 | ‘b110 |
| A1\_5E1\_2E3 (14) | ‘b101 | ‘b100 | A2\_4E1\_E3 (10) | ‘b100 | ‘b100 |
|  |  |  | A2\_5E1 (11) | ‘b001 | ‘b100 |

Adders 1 and 2 states and select signals (easier to copy for the following tables)

Shift=0

|  |  |  |
| --- | --- | --- |
| Adder 1 | | |
| State1 | S1a | S1b |
| A1\_IDLE (0) | ’b111 | ’b111 |
| A1\_E2 (2) | ’b000 | ’b000 |
| A1\_2E2 (3) | ‘b001 | ‘b000 |
| A1\_2E2 (3) | ‘b001 | ‘b000 |
| A1\_E2\_2E3 (1) | ‘b011 | ‘b001 |
| A1\_E2\_2E3 (1) | ‘b011 | ‘b001 |
| A1\_E2\_2E4 (4) | ‘b011 | ‘b011 |
| A1\_2E2\_5E4 (5) | ‘b010 | ‘b010 |
| A1\_IDLE (0) | ’b111 | ’b111 |

|  |  |  |
| --- | --- | --- |
| Adder 2 | | |
| State2 | S2a | S2b |
| A2\_IDLE (0) | ‘b111 | ‘b111 |
| A2\_IDLE (0) | ‘b111 | ‘b111 |
| A2\_2E1\_E3 (1) | ‘b000 | ‘b000 |
| A2\_E1\_2E3 (3) | ‘b001 | ‘b001 |
| A2\_2E2\_E3 (2) | ‘b011 | ‘b000 |
| A2\_2E2\_E4 (4) | ‘b011 | ‘b011 |
| A2\_5E4 (5) | ‘b010 | ‘b011 |
| A2\_4E4\_E2 (7) | ‘b010 | ‘b010 |
| A2\_IDLE (0) | ‘b111 | ‘b111 |

|  |  |
| --- | --- |
| Output muxes | |
| S\_h1 | S\_h2 |
| ‘b00 | ‘b00 |
| ‘b00 | ‘b00 |
| ‘b00 | ‘b00 |
| ‘b01 | ‘b01 |
| ‘b11 | ‘b00 |
| ‘b10 | ‘b00 |
| ‘b11 | ‘b11 |
| ‘b01 | ‘b10 |
| ‘b00 | ‘b00 |

Shift =1

|  |  |  |
| --- | --- | --- |
| Adder 1 | | |
| State1 | S1a | S1b |
| A1\_IDLE (0) | ’b111 | ’b111 |
| A1\_IDLE (0) | ’b111 | ’b111 |
| A1\_IDLE (0) | ’b111 | ’b111 |
| A1\_2E3\_E1 (8) | ‘b110 | ‘b110 |
| A1\_E2\_2E3 (1) | ‘b011 | ‘b001 |
| A1\_E2 (2) | ’b000 | ’b000 |
| A1\_E2\_2E4 (4) | ‘b011 | ‘b011 |
| A1\_IDLE (0) | ’b111 | ’b111 |
| A1\_IDLE (0) | ’b111 | ’b111 |

|  |  |  |
| --- | --- | --- |
| Adder 2 | | |
| State2 | S2a | S2b |
| A2\_IDLE (0) | ‘b111 | ‘b111 |
| A2\_E3 (8) | ‘b110 | ‘b110 |
| A2\_4E1\_E3 (10) | ‘b100 | ‘b100 |
| A2\_2E1\_E3 (1) | ‘b000 | ‘b000 |
| A2\_2E1\_E3 (1) | ‘b000 | ‘b000 |
| A2\_2E2\_E3 (2) | ‘b011 | ‘b000 |
| A2\_2E2\_E4 (4) | ‘b011 | ‘b011 |
| A2\_4E4\_E2 (7) | ‘b010 | ‘b010 |
| A2\_IDLE (0) | ‘b111 | ‘b111 |

|  |  |
| --- | --- |
| Output muxes | |
| S\_h1 | S\_h2 |
| ‘b00 | ‘b00 |
| ‘b00 | ‘b00 |
| ‘b01 | ‘b01 |
| ‘b01 | ‘b10 |
| ‘b00 | ‘b10 |
| ‘b01 | ‘b11 |
| ‘b11 | ‘b10 |
| ‘b10 | ‘b00 |
| ‘b00 | ‘b00 |

Shift=2

|  |  |  |
| --- | --- | --- |
| Adder 1 | | |
| State1 | S1a | S1b |
| A1\_IDLE (0) | ’b111 | ’b111 |
| A1\_IDLE (0) | ’b111 | ’b111 |
| A1\_2E3 (12) | ‘b100 | ‘b000 |
| A1\_5E1\_2E3 (14) | ‘b101 | ‘b100 |
| A1\_5E1\_2E3 (14) | ‘b101 | ‘b100 |
| A1\_2E3\_E1 (8) | ‘b110 | ‘b110 |
| A1\_E2\_2E3 (1) | ‘b011 | ‘b001 |
| A1\_E2\_2E3 (1) | ‘b011 | ‘b001 |
| A1\_E2\_2E4 (4) | ‘b011 | ‘b011 |
| A1\_IDLE (0) | ’b111 | ’b111 |

|  |  |  |
| --- | --- | --- |
| Adder 2 | | |
| State2 | S2a | S2b |
| A2\_IDLE (0) | ‘b111 | ‘b111 |
| A2\_5E1 (11) | ‘b001 | ‘b100 |
| A2\_E3 (8) | ‘b110 | ‘b110 |
| A2\_4E1\_E3 (10) | ‘b100 | ‘b100 |
| A2\_2E1\_E3 (1) | ‘b000 | ‘b000 |
| A2\_2E1\_E3 (1) | ‘b000 | ‘b000 |
| A2\_2E2\_E3 (2) | ‘b011 | ‘b000 |
| A2\_2E2\_E4 (4) | ‘b011 | ‘b011 |
| A2\_IDLE (0) | ‘b111 | ‘b111 |
| A2\_IDLE (0) | ‘b111 | ‘b111 |

|  |  |
| --- | --- |
| Output muxes | |
| S\_h1 | S\_h2 |
| ‘b00 | ‘b00 |
| ‘b00 | ‘b00 |
| ‘b00 | ‘b00 |
| ‘b11 | ‘b00 |
| ‘b00 | ‘b00 |
| ‘b11 | ‘b01 |
| ‘b11 | ‘b00 |
| ‘b10 | ‘b10 |
| ‘b01 | ‘b11 |
| ‘b00 | ‘b00 |

Complete table of all select signals in all shift cases:

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Shift 0 |  | | | | | | | | |
| **Adder 1** | | | **Adder2** | | | **Output muxes** | | **Notes** |
| State1 | S1a | S1b | State2 | S2a | S2b | S\_h1 | S\_h2 | Start @ adder 1  Condition: E2\_ready |
| A1\_IDLE (0) | ’b111 | ’b111 | A2\_IDLE (0) | ‘b111 | ‘b111 | ‘b00 | ‘b00 |
| A1\_E2 (2) | ’b000 | ’b000 | A2\_IDLE (0) | ‘b111 | ‘b111 | ‘b00 | ‘b00 |
| A1\_2E2 (3) | ‘b001 | ‘b000 | A2\_2E1\_E3 (1) | ‘b000 | ‘b000 | ‘b00 | ‘b00 |
| A1\_2E2 (3) | ‘b001 | ‘b000 | A2\_E1\_2E3 (3) | ‘b001 | ‘b001 | ‘b01 | ‘b01 |
| A1\_E2\_2E3 (1) | ‘b011 | ‘b001 | A2\_2E2\_E3 (2) | ‘b011 | ‘b000 | ‘b11 | ‘b00 |
| A1\_E2\_2E3 (1) | ‘b011 | ‘b001 | A2\_2E2\_E4 (4) | ‘b011 | ‘b011 | ‘b10 | ‘b00 |
| A1\_E2\_2E4 (4) | ‘b011 | ‘b011 | A2\_5E4 (5) | ‘b010 | ‘b011 | ‘b11 | ‘b11 |
| A1\_2E2\_5E4 (5) | ‘b010 | ‘b010 | A2\_4E4\_E2 (7) | ‘b010 | ‘b010 | ‘b01 | ‘b10 |
| A1\_IDLE (0) | ’b111 | ’b111 | A2\_IDLE (0) | ‘b111 | ‘b111 | ‘b01 | ‘b10 |
| Shift 1 |  | | | | | | | | |
| **Adder 1** | | | **Adder 2** | | | **Output muxes** | | **Notes** |
| State1 | S1a | S1b | State2 | S2a | S2b | S\_h1 | S\_h2 | Start @ adder 2  Condition: E3\_ready |
| A1\_IDLE (0) | ’b111 | ’b111 | A2\_IDLE (0) | ‘b111 | ‘b111 | ‘b00 | ‘b00 |
| A1\_IDLE (0) | ’b111 | ’b111 | A2\_E3 (8) | ‘b110 | ‘b110 | ‘b00 | ‘b00 |
| A1\_IDLE (0) | ’b111 | ’b111 | A2\_4E1\_E3 (10) | ‘b100 | ‘b100 | ‘b01 | ‘b01 |
| A1\_2E3\_E1 (8) | ‘b110 | ‘b110 | A2\_2E1\_E3 (1) | ‘b000 | ‘b000 | ‘b01 | ‘b10 |
| A1\_E2\_2E3 (1) | ‘b011 | ‘b001 | A2\_2E1\_E3 (1) | ‘b000 | ‘b000 | ‘b00 | ‘b10 |
| A1\_E2 (2) | ’b000 | ’b000 | A2\_2E2\_E3 (2) | ‘b011 | ‘b000 | ‘b01 | ‘b11 |
| A1\_E2\_2E4 (4) | ‘b011 | ‘b011 | A2\_2E2\_E4 (4) | ‘b011 | ‘b011 | ‘b11 | ‘b10 |
| A1\_IDLE (0) | ’b111 | ’b111 | A2\_4E4\_E2 (7) | ‘b010 | ‘b010 | ‘b10 | ‘b00 |
| A1\_IDLE (0) | ’b111 | ’b111 | A2\_IDLE (0) | ‘b111 | ‘b111 | ‘b10 | ‘b00 |
| Shift 2 | Condition could be E1\_ready instead but it’s easier to control with E2\_ready (go signals) | | | | | | | | |
| **Adder 1** | | | **Adder 2** | | | **Output muxes** | | **Notes** |
| State1 | S1a | S1b | State2 | S2a | S2b | S\_h1 | S\_h2 | Start @ adder 2  Condition: E2\_ready |
| A1\_IDLE (0) | ’b111 | ’b111 | A2\_IDLE (0) | ‘b111 | ‘b111 | ‘b00 | ‘b00 |
| A1\_IDLE (0) | ’b111 | ’b111 | A2\_5E1 (11) | ‘b001 | ‘b100 | ‘b00 | ‘b00 |
| A1\_2E3 (12) | ‘b100 | ‘b000 | A2\_E3 (8) | ‘b110 | ‘b110 | ‘b00 | ‘b00 |
| A1\_5E1\_2E3 (14) | ‘b101 | ‘b100 | A2\_4E1\_E3 (10) | ‘b100 | ‘b100 | ‘b11 | ‘b00 |
| A1\_5E1\_2E3 (14) | ‘b101 | ‘b100 | A2\_2E1\_E3 (1) | ‘b000 | ‘b000 | ‘b00 | ‘b00 |
| A1\_2E3\_E1 (8) | ‘b110 | ‘b110 | A2\_2E1\_E3 (1) | ‘b000 | ‘b000 | ‘b11 | ‘b01 |
| A1\_E2\_2E3 (1) | ‘b011 | ‘b001 | A2\_2E2\_E3 (2) | ‘b011 | ‘b000 | ‘b11 | ‘b00 |
| A1\_E2\_2E3 (1) | ‘b011 | ‘b001 | A2\_2E2\_E4 (4) | ‘b011 | ‘b011 | ‘b10 | ‘b10 |
| A1\_E2\_2E4 (4) | ‘b011 | ‘b011 | A2\_IDLE (0) | ‘b111 | ‘b111 | ‘b01 | ‘b11 |
| A1\_IDLE (0) | ’b111 | ’b111 | A2\_IDLE (0) | ‘b111 | ‘b111 | ‘b01 | ‘b11 |
|  | | | | | | | | |

Testing :

Starts from 2nd row.

Complete table of all select signals in all shift cases: **UPDATED**, no E2\_ready , all wait for E3\_ready

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Shift 0 | S1a, S2a, S1b, S2b with the start, S\_h1 & S\_h2 with the end so that output is ready | | | | | | | | |
| **Adder 1** | | | **Adder2** | | | **Output muxes** | | **Notes** |
| State1 | S1a | S1b | State2 | S2a | S2b | S\_h1 | S\_h2 | Need: 6 s\_h black values |
| A1\_IDLE (0) | ’b111 | ’b111 | A2\_IDLE (0) | ‘b111 | ‘b111 | ‘b00 | ‘b00 |
| A1\_E2 (2) | ’b000 | ’b000 | A2\_2E1\_E3 (1) | ‘b000 | ‘b000 | ‘b00 | ‘b00 |
| A1\_2E2 (3) | ‘b001 | ‘b000 | A2\_E1\_2E3 (3) | ‘b001 | ‘b001 | ‘b01 | ‘b01 |
| A1\_E2\_2E3 (1) | ‘b011 | ‘b001 | A2\_2E2\_E3 (2) | ‘b011 | ‘b000 | ‘b11 | ‘b00 |
| A1\_E2\_2E3 (1) | ‘b011 | ‘b001 | A2\_2E2\_E4 (4) | ‘b011 | ‘b011 | ‘b10 | ‘b00 |
| A1\_E2\_2E4 (4) | ‘b011 | ‘b011 | A2\_5E4 (5) | ‘b010 | ‘b011 | ‘b11 | ‘b11 |
| A1\_2E2\_5E4 (5) | ‘b010 | ‘b010 | A2\_4E4\_E2 (7) | ‘b010 | ‘b010 | ‘b01 | ‘b10 |
| A1\_IDLE (0) | ’b111 | ’b111 | A2\_IDLE (0) | ‘b111 | ‘b111 | ‘b01 | ‘b10 |
| Shift 1 |  | | | | | | | | |
| **Adder 1** | | | **Adder 2** | | | **Output muxes** | | **Notes** |
| State1 | S1a | S1b | State2 | S2a | S2b | S\_h1 | S\_h2 |  |
| A1\_IDLE (0) | ’b111 | ’b111 | A2\_IDLE (0) | ‘b111 | ‘b111 | ‘b00 | ‘b00 |
| A1\_IDLE (0) | ’b111 | ’b111 | A2\_E3 (8) | ‘b110 | ‘b110 | ‘b00 | ‘b00 |
| A1\_IDLE (0) | ’b111 | ’b111 | A2\_4E1\_E3 (10) | ‘b100 | ‘b100 | ‘b01 | ‘b01 |
| A1\_2E3\_E1 (8) | ‘b110 | ‘b110 | A2\_2E1\_E3 (1) | ‘b000 | ‘b000 | ‘b01 | ‘b10 |
| A1\_E2\_2E3 (1) | ‘b011 | ‘b001 | A2\_2E1\_E3 (1) | ‘b000 | ‘b000 | ‘b00 | ‘b10 |
| A1\_E2 (2) | ’b000 | ’b000 | A2\_2E2\_E3 (2) | ‘b011 | ‘b000 | ‘b01 | ‘b11 |
| A1\_E2\_2E4 (4) | ‘b011 | ‘b011 | A2\_2E2\_E4 (4) | ‘b011 | ‘b011 | ‘b11 | ‘b10 |
| A1\_IDLE (0) | ’b111 | ’b111 | A2\_4E4\_E2 (7) | ‘b010 | ‘b010 | ‘b10 | ‘b00 |
| A1\_IDLE (0) | ’b111 | ’b111 | A2\_IDLE (0) | ‘b111 | ‘b111 | ‘b10 | ‘b00 |
| Shift 2 |  | | | | | | | | |
| **Adder 1** | | | **Adder 2** | | | **Output muxes** | | **Notes** |
| State1 | S1a | S1b | State2 | S2a | S2b | S\_h1 | S\_h2 | Start @ adder2, cond:E3\_ready  Adder1 starts 1 clk after |
| A1\_IDLE (0) | ’b111 | ’b111 | A2\_IDLE (0) | ‘b111 | ‘b111 | ‘b00 | ‘b00 |
| A1\_IDLE (0) | ’b111 | ’b111 | A2\_5E1 (11) | ‘b001 | ‘b100 | ‘b00 | ‘b00 |
| A1\_2E3 (12) | ‘b100 | ‘b000 | A2\_E3 (8) | ‘b110 | ‘b110 | ‘b00 | ‘b00 |
| A1\_5E1\_2E3 (14) | ‘b101 | ‘b100 | A2\_4E1\_E3 (10) | ‘b100 | ‘b100 | ‘b11 | ‘b00 |
| A1\_5E1\_2E3 (14) | ‘b101 | ‘b100 | A2\_2E1\_E3 (1) | ‘b000 | ‘b000 | ‘b00 | ‘b00 |
| A1\_2E3\_E1 (8) | ‘b110 | ‘b110 | A2\_2E1\_E3 (1) | ‘b000 | ‘b000 | ‘b11 | ‘b01 |
| A1\_E2\_2E3 (1) | ‘b011 | ‘b001 | A2\_2E2\_E3 (2) | ‘b011 | ‘b000 | ‘b11 | ‘b00 |
| A1\_E2\_2E3 (1) | ‘b011 | ‘b001 | A2\_2E2\_E4 (4) | ‘b011 | ‘b011 | ‘b10 | ‘b10 |
| A1\_E2\_2E4 (4) | ‘b011 | ‘b011 | A2\_IDLE (0) | ‘b111 | ‘b111 | ‘b01 | ‘b11 |
| A1\_IDLE (0) | ’b111 | ’b111 | A2\_IDLE (0) | ‘b111 | ‘b111 | ‘b01 | ‘b11 |
|  | | | | | | | | |

Testing :

Starts from 2nd row.

Load\_sel (comb. signal to load the registers containing s\_h1 and s\_h2 values) needs to be on 2 clks before the output is on the output port, 1 clk